

# Design and Implementation of High Speed 16x16 CMOS Vedic Multiplier

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**Abstract**— In today scenario digital circuits are become more and more complex because of long arithmetic calculations but with the help of Vedic mathematics that calculations can become easy and fast. To make multiplier we have different techniques, in this paper we design 16x16 CMOS multiplier using Vedic mathematics technique.

**Keywords**—Multiplier, Vedic Mathematics, CMOS, 16x16 multiplier.

## I. INTRODUCTION

The word ‘Vedic’ is derived from the word ‘Veda’ which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc. In this paper, Urdhva Tiryakbhyam Sutra is first applied to the binary number system and is used to develop digital multiplier architecture. This is shown to be very similar to the popular array multiplier architecture. This Sutra also shows the effectiveness of to reduce the NXN multiplier structure into an efficient 4X4 multiplier structures. The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics. Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm) for high speed multiplication, and less number of transistor count. An adiabatic logic is used to design 16X16 CMOS Vedic multiplier [1].

## II. BASIC OF VEDIC MULTIPLIER

The Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one [2]. This is

so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works.

## III. DESIGN AND IMPLEMENTATION OF VEDIC MULTIPLIER

The designing of Vedic Multiplier is based on a novel technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift. Where small blocks are used to design the bigger one.

### 3.1 AND Gate

The AND gate is a basic digital logic gate that implements logical conjunction it behaves according to the truth table to the right. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results.

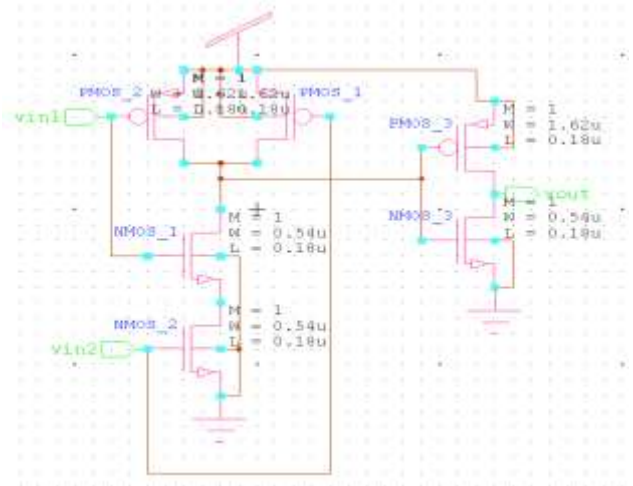


Fig.3.1. Circuit diagram of AND gate

### 3.2 XOR Gate

The XOR gate performs an exclusive –OR operation on the inputs. Exclusive –OR produces a 1 output if one (but only one) input is 1. If both operands are 0, the output is 0. Likewise, if both operands are 1, the output is also 0.

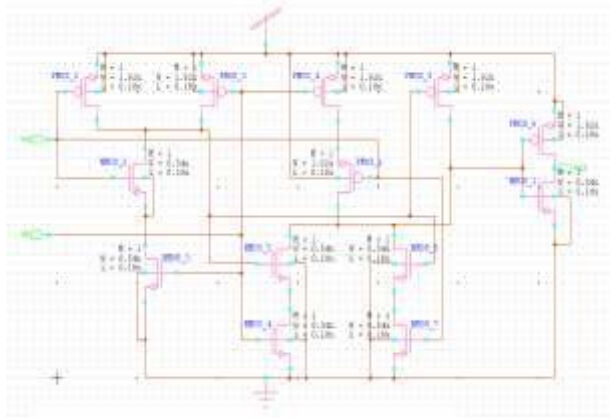


Fig.3.2. Circuit diagram of XOR gate

### 3.3 Full Adder

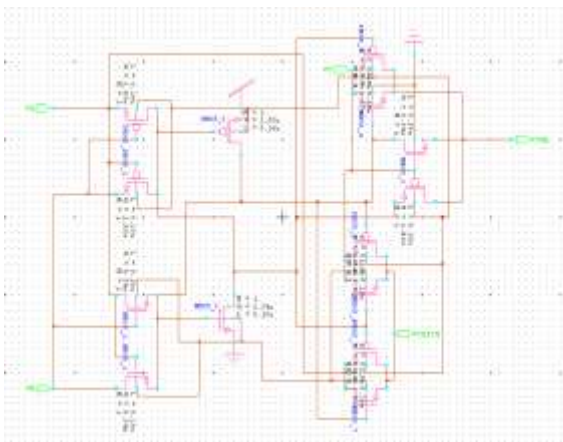


Fig.3.3. Circuit diagram of full adder

### 3.4 Design of 4x4 Vedic Multiplier

Let's analyze 4x4 multiplications [3], say A3A2A1A0 and B3B2B1B0. Following are the output line for the multiplication result, Q7Q6Q5Q4Q3Q2Q1Q0 [4]. Block diagram of 4x4 Vedic Multiplier is given below

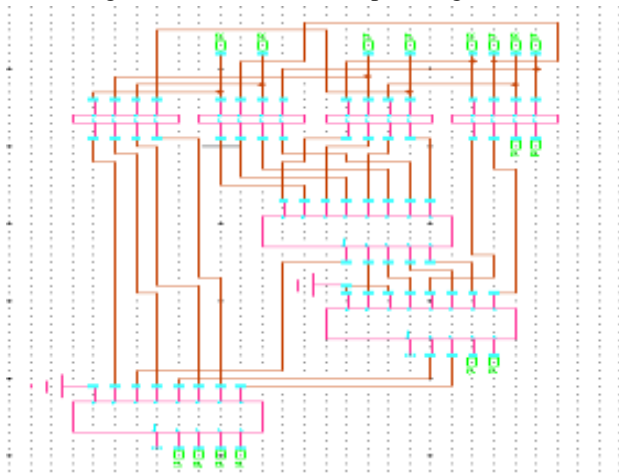


Fig.3.4: Circuit Diagram of 4x4 Bit Vedic Multiplier

### 3.5 Design of 8x8 Vedic Multiplier

Now the basic building block of 8x8 bit Vedic multiplier is 4x4 bits multiplier. For bigger multiplier implementation like 8x8 bits 5multiplier the 4x4 bits multiplier units has been used as components which are implemented already in Tanner library [5]. The structural modeling of any design shows fastest design.

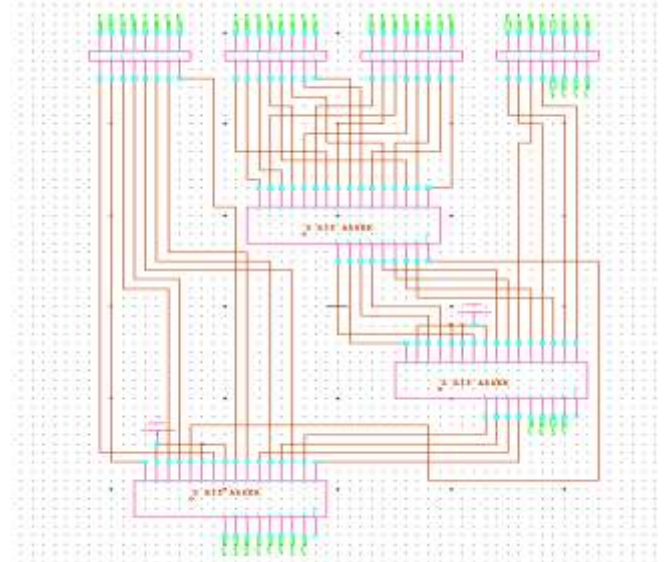


Fig.3.5: Block diagram of 8x8 Vedic Multiplier

### 3.6 Design of 16x16 Vedic Multiplier

The 16X16 bit multiplier structured using 8X8 bits blocks as shown below. The 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL [6]. The outputs of 8X8 bit multipliers are added accordingly to obtain the 32 bits final product. Thus, in the final stage two adders are also required. Similarly, we have extended same for input bits 32, 64.

$$\text{RESULT} = (Q_{31} - Q_{16}) \& (Q_{15} - Q_{8}) \& (Q_{7} - Q_{0})$$

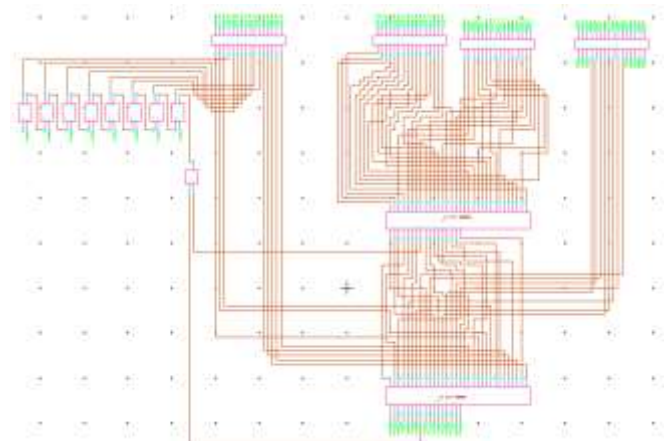


Fig.3.6: Block diagram of 16x16 Vedic Multiplier

## IV. RESULT AND ANALYSIS

Simulation result and analysis of individual component used to design vedic multiplier is discussed below. Vedic

multiplier is designed by means of 180nm CMOS technology.

#### 4.1 AND Gate

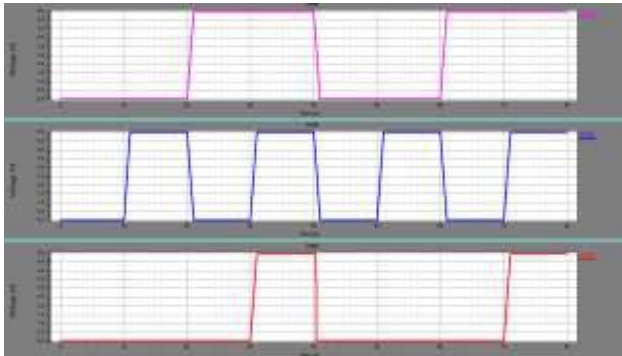


Fig. 4.1 Waveform of AND gate

#### 4.2 XOR Gate



Fig. 4.2 Waveform of XOR gate

#### 4.3 Full Adder

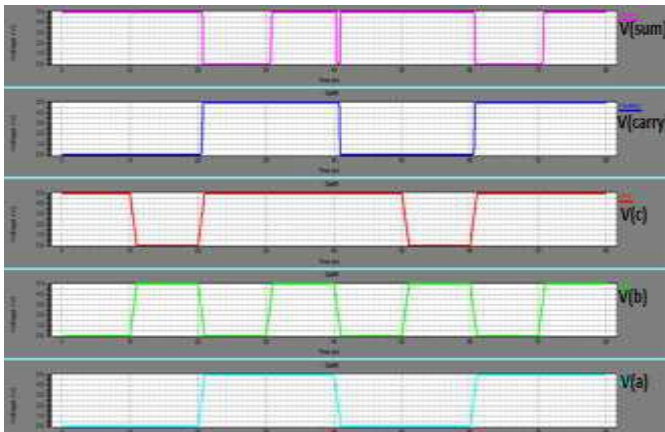


Fig. 4.3. Output Waveform of Full adder

#### 4.4 Simulation Results Of 2x2 Vedic Multiplier

When the given input bit  $A=a_1a_0$  &  $B=b_1b_0$   
 Where  $A = 3$  (0011) &  $B = 3$  (0011)  
 then its output  $S = 9$  (1001)  
 which is shown in given below:  
 When the given input bit  $A=a_1a_0$  &  $B=b_1b_0$

Where  $A = 3$  (0011) &  $B = 3$  (0011)  
 then its output  $S = 9$  (1001)  
 which is shown in given below:

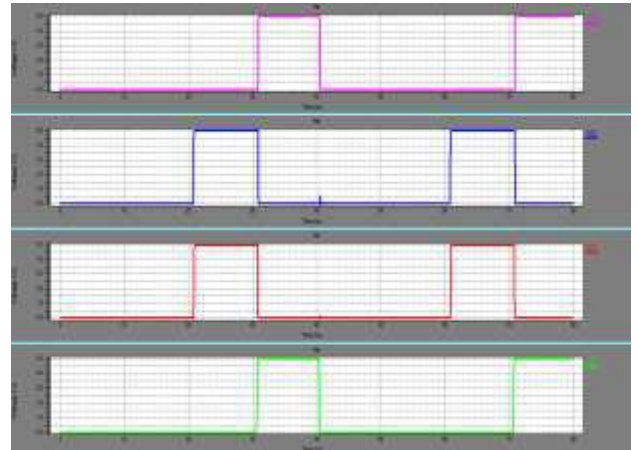


Fig.4.4: Output waveform of 2x2 vbedic multiplier

#### 4.5 Simulation Results Of 4x4 Vedic Multiplier

When The given Input Bit  $A=A_3a_2a_1a_0$  &  $B=B_3b_2b_1b_0$   
 Then  $S = S_7s_6s_5s_4s_3s_2s_1s_0$   
 $A=15$ (1111)  
 $B=15$ (1111)  
 Then Output Its  $S = 225$  (11100001)

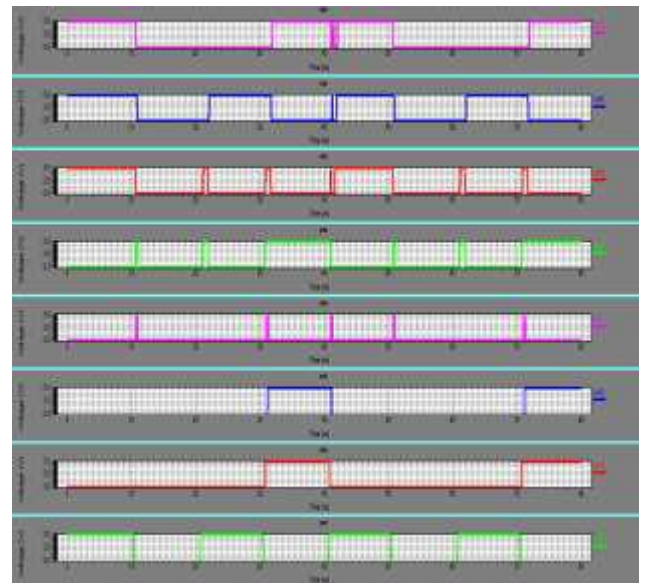


Fig.4.5: Output waveform of 4x4 vbedic multiplier

#### 4.6 Simulation Results Of 8x8 Cmos Vedic Multiplier

When the given input bit  $A=a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0$  &  $B = b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0$   
 $A=255$ (1111 1111)  
 $B=15$ (1111 1111)  
 Then output its  $S = 65,025$  (1111 1110 0000 0001)

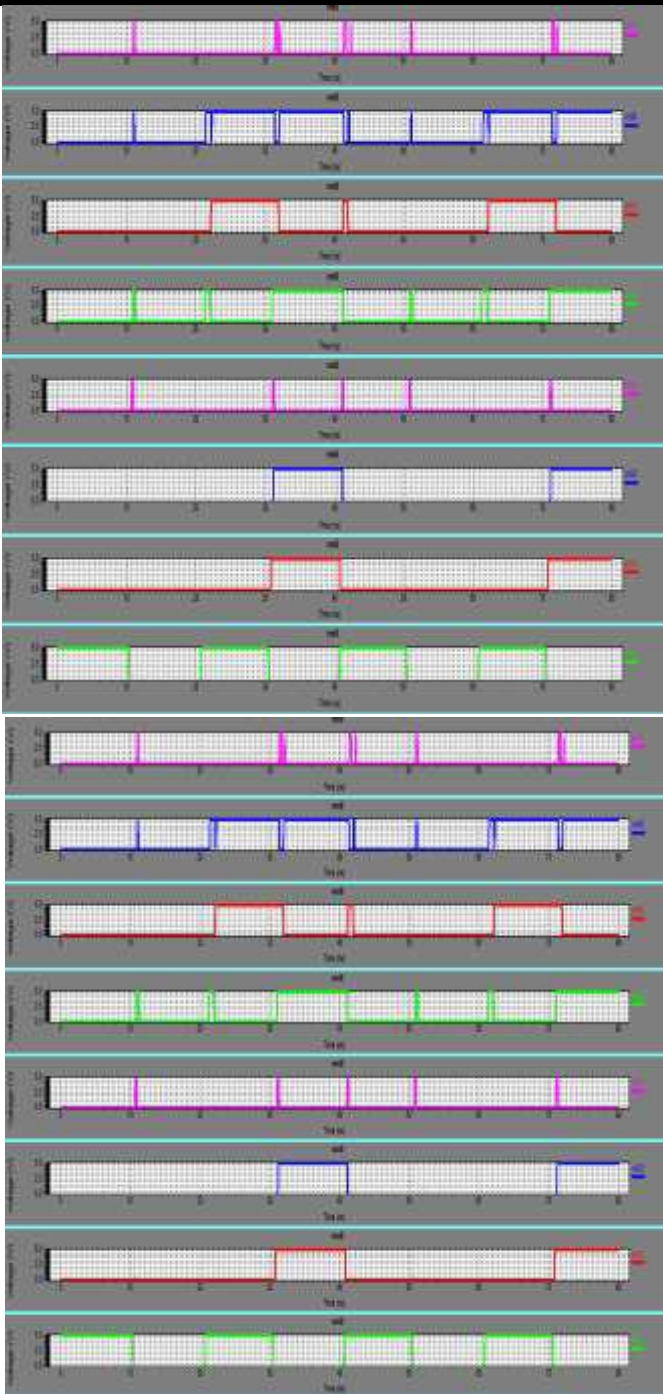


Fig.4.6: Output waveform of 8x8 vbedic multiplier

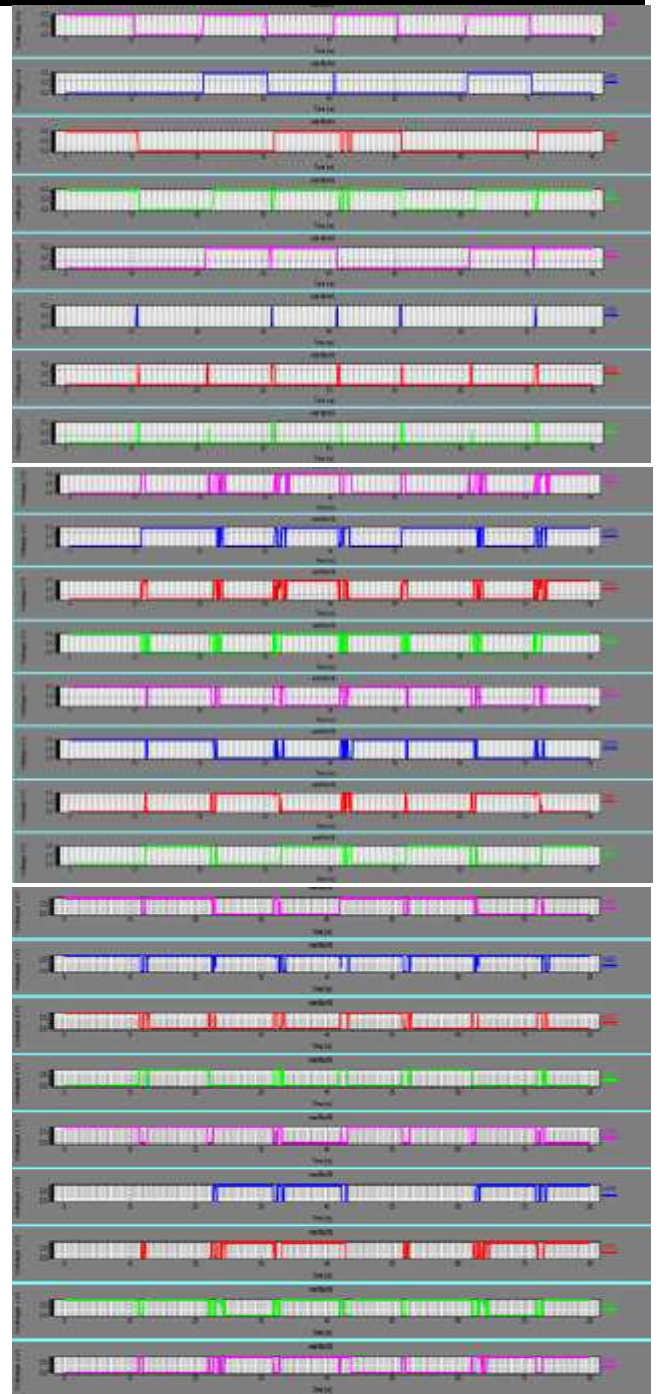


Fig.4.7: Output waveform of 16x16 vedic multiplier

#### 4.7 Simulation Results Of 8x8 Cmos Vedic Multiplier

When the given input bit A=a15 a14 a13 a12 a11 a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0 & B = b15 b14 b13 b12 b11 b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0  
 A=65,535 (1111 1111 1111 1111)  
 B=65,535(1111 1111 1111 1111)  
 Then output its S = 65,025 (1111 1111 1111 1110 0000 0000 0000 0001)  
 which is shown in given below:

#### V. COMPARISON OF PROPOSED 16X16 CMOS VEDIC MULTIPLIER WITH EXISTING 16X16 VEDIC MULTIPLIER

Analysis of delay and power of vedic multiplier at different  $V_{DD}$  is shown in table 5.1

$V_{DD}$ (V)	Existing 16x16 vedic multiplier		Proposed 16x16 vedic multiplier	
	Delay Time (ns)	Power (mW)	Delay Time (ns)	Power (mW)
1.8	25.871	15.813	20.856	12.878
2	22.564	18.970	17.580	13.524

3	20.430	21.549	16.158	14.441
4	15.791	25.674	12.020	17.856
5	12.654	28.47	9.087	19.587

## VI. CONCLUSION

The design of 16x16 CMOS Vedic multiplier has been implemented on Tanner EDA tool 13.00v. The computation delay for 8x8 bits Vedic multiplier is 9.203 ns at 5V and for 16x16 CMOS Vedic multiplier is 9.087 ns at 5V. Since power and delay of proposed Vedic multiplier is reduced as compared to existing multiplier. Thus, it is more efficient for fast multiplication.

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